CLAIMS

I/We claim:

[c1] 1. A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:

a semiconductor substrate;

a gate oxide formed on said semiconductor substrate;

a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into said gate structure;

an isolation layer formed over the sidewall of said gate structure;

first spacers formed on the sidewall of said isolation layer and filled into said undercut structure for storing carriers;

source and drain regions formed adjacent to said gate structure and under said undercut structure; and

salicide formed on said gate structure and said source and drain regions.

[c2] 2. The nonvolatile memory of Claim 1, further comprising pocket ion implantation region located adjacent to said source and drain regions and under said undercut structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.

[c3] 3. The nonvolatile memory of Claim 1, further comprising:

lightly doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said lightly doped drain region is shallower than the one of said source and drain regions and said lightly doped drain region is closer to the channel under said gate structure than said source and drain regions; and

pocket ion implantation region adjacent to said lightly doped drain regions, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.

[c4] 4. The nonvolatile memory of Claim 1, further comprising:

double doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said double doped drain region is deeper than the one of said source and drain regions and said double doped drain region is closer to the channel under said gate structure than said source and drain regions; and

pocket ion implantation region adjacent to said double doped drain region and under said undercut structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.

[c5] 5. The nonvolatile memory of Claim 1, wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate and said undercut-filling material are formed of oxide or the material having energy gap larger than 7eV.

[c6] 6. The nonvolatile memory of Claim 2, wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate and said undercut-filling material are formed of oxide or the material having energy gap larger than 7eV.

[c7] 7. The nonvolatile memory of Claim 3, wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said

gate and said undercut-filling material are formed of oxide or the material having energy gap larger than 7eV.

[c8] 8. The nonvolatile memory of Claim 4, wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate and said undercut-filling material are formed of oxide or the material having energy gap larger than 7eV.

[c9] 9. The nonvolatile memory of Claim 1, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide or the material having energy gap larger than 7eV.

[c10] 10. The nonvolatile memory of Claim 2, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide or the material having energy gap larger than 7eV.

[c11] 11. The nonvolatile memory of Claim 3, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide or the material having energy gap larger than 7eV.

[c12] 12. The nonvolatile memory of Claim 4, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide or the material having energy gap larger than 7eV.

[c13] 13. The nonvolatile memory of Claim 1, wherein said isolation layer is formed of oxide or the material having energy gap larger than 7eV.

[c14] 14. The nonvolatile memory of Claim 1, wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

[c15] 15. The nonvolatile memory of Claim 1, wherein said silicide material includes $TiSi_2$, $CoSi_2$ or NiSi.

[c16] 16. The nonvolatile memory of Claim 2, wherein said isolation layer is formed of oxide or the material having energy gap larger than 7eV.

[c17] 17. The nonvolatile memory of Claim 2, wherein said wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

[c18] 18. The nonvolatile memory of Claim 2, wherein said silicide material includes $TiSi_2$, $CoSi_2$ or NiSi.

[c19] 19. The nonvolatile memory of Claim 3, wherein said isolation layer is formed of oxide or the material having energy gap larger than 7eV.

[c20] 20. The nonvolatile memory of Claim 3, wherein said wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

[c21] 21. The nonvolatile memory of Claim 3, wherein said silicide material includes $TiSi_2$, $CoSi_2$ or NiSi.

[c22] 22. The nonvolatile memory of Claim 4, wherein said isolation layer is formed of oxide or the material having energy gap larger than 7eV.

[c23] 23. The nonvolatile memory of Claim 4, wherein said wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

[c24] 24. The nonvolatile memory of Claim 4, wherein said silicide material includes $TiSi_2$, $CoSi_2$ or NiSi.

[c25] 25. A nonvolatile memory with undercut trapping structure, said nonvolatile memory comprising:

a semiconductor substrate;

a gate oxide formed on said semiconductor substrate;

a gate structure formed on said gate oxide, wherein said gate structure including a undercut structure formed at lower portion of the gate structure and inwardly into said gate structure, wherein said gate structure comprising a stacked structure including of polysilsicon layer/silicide layer and a first dielectric layer;

a second dielectric layer formed over the sidewall of said gate structure;

first spacers formed on the sidewall of said second dielectric layer and filled into said undercut structure for storing carriers; and

source and drain regions formed adjacent to said gate structure and under said undercut structure.

[c26] 26. The nonvolatile memory of Claim 25, further comprising pocket ion implantation region located adjacent to said source and drain regions and under said undercut structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.

[c27] 27. The nonvolatile memory of Claim 25, further comprising:

lightly doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said lightly doped drain region is shallower than the one of said source and drain regions and said lightly doped drain region is closer to the channel under said gate structure than said source and drain regions; and

pocket ion implantation region adjacent to said lightly doped drain regions, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.

[c28] 28. The nonvolatile memory of Claim 25, further comprising:

double doped drain region adjacent to said source and drain regions and under said undercut structure, wherein the junction of said double doped drain region is deeper than the one of said source and drain regions and said double doped drain region is closer to the channel under said gate structure than said source and drain regions; and

pocket ion implantation region adjacent to said double doped drain region and under said undercut structure, wherein the conductive type of the pocket ion implantation region is opposite to the one of the source and drain regions.

[c29] 29. The nonvolatile memory of Claim 25, wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate and said undercut-filling material are formed of oxide or the material having energy gap larger than 7eV.

[c30] 30. The nonvolatile memory of Claim 26, wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate and said undercut-filling material are formed of oxide or the material having energy gap larger than 7eV.

[c31] 31. The nonvolatile memory of Claim 27, wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate and said undercut-filling material is formed of oxide or the material having energy gap larger than 7eV.

[c32] 32. The nonvolatile memory of Claim 28, wherein the undercut-filling material filled into said undercut structure includes nitride or the material having energy gap lower than 6eV, said first spacers attached onto the sidewall of said gate and said undercut-filling material are formed of oxide or the material having energy gap larger than 7eV.

[c33] 33. The nonvolatile memory of Claim 25, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide or the material having energy gap larger than 7eV.

[c34] 34. The nonvolatile memory of Claim 26, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide or the material having energy gap larger than 7eV.

[c35] 35. The nonvolatile memory of Claim 27, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide or the material having energy gap larger than 7eV.

[c36] 36. The nonvolatile memory of Claim 28, further comprising second spacers attached on said first spacers, wherein said second spacers are formed of oxide or the material having energy gap larger than 7eV.

[c37] 37. The nonvolatile memory of Claim 25, wherein said second dielectric layer is formed of oxide or the material having energy gap larger than 7eV.

[c38] 38. The nonvolatile memory of Claim 25, wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

[c39] 39. The nonvolatile memory of Claim 25, wherein said silicide material includes $TiSi_2$, WSi_2 $CoSi_2$ or NiSi.

[c40] 40. The nonvolatile memory of Claim 25, wherein said first dielectric layer is formed of oxide, nitride or the combination of oxide and nitride layers.

[c41] 41. The nonvolatile memory of Claim 26, wherein said wherein said second dielectric layer is formed of oxide or the material having energy gap larger than 7eV.

[c42] 42. The nonvolatile memory of Claim 26, wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

[c43] 43. The nonvolatile memory of Claim 26, wherein said silicide material includes $TiSi_2$,, WSi_2, $CoSi_2$ or NiSi.

[c44] 44. The nonvolatile memory of Claim 26, wherein said first dielectric layer is formed of oxide, nitride or the combination of oxide and nitride layers.

[c45] 45. The nonvolatile memory of Claim 27, wherein said wherein said second dielectric layer is formed of oxide or the material having energy gap larger than 7eV.

[c46] 46. The nonvolatile memory of Claim 27, wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

[c47] 47. The nonvolatile memory of Claim 27, wherein said silicide material includes $TiSi_2$, WSi_2, $CoSi_2$ or NiSi.

[c48] 48. The nonvolatile memory of Claim 27, wherein said first dielectric layer is formed of oxide, nitride or the combination of oxide and nitride layers.

[c49] 49. The nonvolatile memory of Claim 28, wherein said wherein said second dielectric layer is formed of oxide or the material having energy gap larger than 7eV.

[c50] 50. The nonvolatile memory of Claim 28, wherein said first spacers are formed of nitride or the material having energy gap lower than 6eV.

[c51] 51. The nonvolatile memory of Claim 28, wherein said silicide material includes $TiSi_2$, ,WSi_2, $CoSi_2$ or NiSi.

[c52] 52. The nonvolatile memory of Claim 28, wherein said first dielectric layer is formed of oxide, nitride or the combination of oxide and nitride layers.